REMARKS

Claims 8 and 17 have been amended. Claims 1-7 and 23 have been cancelled without prejudice to focus on method claims 8-22. Claims 8-22 are pending in the application. Applicant respectfully requests reconsideration.

Claim Objections

Claims 8-22 were objected to because of the following informalities:

It is not clear what the Applicant intend to mean by claiming "processor programmed **into** said programmable logic device."

Independent claim 8 has been amended to recite "programming said processor types into said at least one programmable logic device such that said at least one programmable logic device is programmed to implement said processor types" (emphasis added). Claim 8, as amended, makes clear that the programmable logic device is programmed to implement said processor types. Therefore, Applicant submits that the meaning of "programming said processor types into said at least one programmable logic device" is clear, and the objection has been overcome.

Independent claim 17 has been amended in a similar manner as claim 8, and therefore overcomes the objection for the reasons given above.

Claim Rejections under 35 U.S.C. § 102

Claims 8-22 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hoare et al. (U.S. Patent Application Publication 20020133325). Applicant respectfully traverses.

Claim 8 is patentable because Hoare fails to disclose, teach or suggest "mapping the user design into operations for execution; partitioning each of said operations into processor types suitable for each of said operations" **and** "programming said processor types into said at least one programmable logic device such that said at least one programmable logic device is programmed to implement said processor types." (emphasis added).

Hoare discloses a discrete event simulator for simulating a circuit comprising four different types of simulation engines: a logic simulation engine, a memory simulation engine, a behavioral simulation engine, and a interconnection and net-list/annotation simulation engine (Hoare, paragraphs [0111], [0112], [0115], and [0117]). The simulator also comprises an event scheduler for scheduling events among the different simulation engines. To simulate a circuit, the circuit is partitioned into four functionally different types of logic representations (gate logic, memory, behavioral, and interconnections), which are mapped to the different types of simulation engines to perform the simulation (Hoare, paragraph [0123]).

However, nowhere does Hoare disclose, teach or suggest programming the processors of the simulation engines into a programmable logic device such that the programmable logic device is programmed to implement the processors of the simulation engines[1]. While discussing the use of programmable logic devices in the context of hardware logic emulators (Hoare, paragraphs [0080], [0102] and [0103]), Hoare does not disclose using a programmable logic device in the discrete event simulator, much less programming the processors of the simulation engines into a

1 The Office Action relies on the processors within the simulation engines as disclosing the processor types.

programmable logic device. If anything, Hoare teaches away from programming the processors of the simulation engines into a programmable logic device. This is because Hoare states that "hardware emulators can only emulate, not simulate, and they lack the functionality of correctly simulating the circuit's characteristics given by the designer's intention and/or target technology." (emphasis added) (Hoare, paragraph [0103]). Because the purpose of the simulation engines is to simulate and Hoare states that hardware emulators lack the functionality to correctly simulate, Hoare teaches away from programming the processors of the simulation engines into a programmable logic device. Since Hoare does not disclose, teach or suggest programming the processors of the simulation engines into a programmable logic device, the simulation engines of Hoare cannot possibly disclose partitioning the operations of a circuit design into processor types **and** "programming the processor types into a programmable logic device such that the programmable logic device is programmed to implement the processor types," as required by claim 8.

By programming the processor types into a programmable logic device instead of using dedicated (fixed) processors, the method of claim 8 enables a verification system to select the processor types best suited for verifying the operations of a particular user design and to program the selected processor types into the programmable logic device. Hoare does not disclose, teach or suggest programming the processors of the simulation engines into a programmable logic device, and therefore does not provide this advantage. In fact, Hoare discloses the logic simulation engine using a "full custom architecture", which is consistent with dedicated processors (Hoare, paragraph [0111]). Further, Hoare teaches away from programming the

processors of the simulation engines into programmable logic devices as explained above.

Claim 8 is also not disclosed, taught or suggested by the hardware logic emulator discussed in Hoare, in which a circuit design is transformed into a gate level design, instead of processor types, and the gate level design is mapped into a programmable logic device (Hoare, paragraphs [0079] and [0080]).

For at least the reasons given above, Applicant submits that independent claim 8 is patentable over Hoare, and respectfully requests that the rejection of claim 8 be withdrawn.

Claims 9-16 depend from claim 8, and are therefore patentable for at least the reasons given for claim 8.

Claim 17 is patentable because Hoare fails to disclose, teach or suggest compiling an electronic design into logic processors, a macro processor, and a memory processor and programming the logic processors, macro processor and memory processor into a programmable logic device such that the programmable logic is programmed to implement these processors, as required by claim 17. As explained above with regard to claim 8, Hoare does not disclose, teach or suggest programming the processors of the simulation engines into a programmable logic device. Therefore, Applicant submits that claim 17 is patentable over Hoare, and respectfully requests that the rejection of claim 17 be withdrawn.

Claims 18-22 depend from claim 17, and are therefore patentable for at least the reasons given for claim 17.

Conclusion

For at least the reasons set forth above, it is submitted that claims 8-22 are in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is encouraged to contact the undersigned at (949) 567-6700 if there is any way to expedite the prosecution of the present application.

Respectfully submitted,

Orrick, Herrington & Sutcliffe LLP

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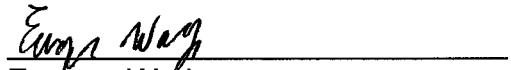
By: 
Eugene Worley
Reg. No. 47,186

Orrick, Herrington & Sutcliffe LLP
4 Park Plaza, Suite 1600
Irvine, California 92614-2558
Telephone: (949) 567-6700
Facsimile: (949) 567-6710